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(54) **Process for producing multilevel metallization in an integrated circuit**

(57) A method for fabricating a multi-level integrated circuit is disclosed which utilizes a grid pattern from which portions corresponding to the metal layer are selectively removed to form a mask which is subsequently

used to deposit dummy features in the open areas between metal lines, thereby to allow the deposition of a substantially planar dielectric surface over the metal layers and dummy features.

EP 0 712 156 A3



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EUROPEAN SEARCH REPORT

Application Number
EP 95 30 7802

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 130 (E-502), 23 April 1987 & JP 61 276345 A (OKI ELECTRIC IND CO LTD), 6 December 1986, * abstract *		H01L21/768
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 046 (E-711), 2 February 1989 & JP 63 240045 A (MATSUSHITA ELECTRIC IND CO LTD), 5 October 1988, * abstract *		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		12 September 1997	Schuermans, N
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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